providing bias_mid to an input electrode of the first semiconductor device such that the first semiconductor device will turn off when bias_mid - V_{DDO} exceeds the threshold of the first semiconductor device; and

actuating a switch in response to the turn off of the first semiconductor device to couple Vpad to bias_mid.

cont. a1

6. The method of claim 5 wherein using the turn off of the first semiconductor device to couple Vpad to bias_mid further comprises:

turning on a second semiconductor device and turning off a third semiconductor device which are coupled together thereby providing a turn on voltage for a fourth semiconductor device; and

using the turn on of the fourth semiconductor device to couple Vpad to bias_mid.

REMARKS

Claims 1-6 are currently pending in this application. Claims 3 and 4 have been amended for clarity, and claims 7-22 have been cancelled without prejudice in response to a restriction requirement. In view of the above amendments and following remarks, applicant respectfully submits that the application is in condition for allowance. Applicant therefore, respectfully requests reexamination, reconsideration and allowance of the application.

The Examiner objected to the drawings filed on January 9, 2002 for including non-conventional symbols and for being hand drawn in part. Applicant submitted formal drawings July 26, 2002 that incorporated conventional symbols in place of the unconventional symbols and replaced the objected to hand drawn figures. In addition, Applicant submits herewith corrected FIGS. 9A, 10, 11A, 14 and 18 that include labels within the previously unmarked boxes. More specifically box 901 has been labeled as a switching circuit as

defined in the originally filed application at page 12, line 34, box 407 has been labeled as a first bias circuit as defined on page 10, line 34 and box 901 has been labeled as a coupling switch as defined on page 17 lines 13-15. Applicant respectfully submits that no new matter has been added and requests that these proposed drawing changes be entered and the objection to the drawings withdrawn.

The Examiner rejected claims 1-6 under 35 U.S.C. 102(b) as being anticipated by Takiba et al. (U.S. Patent 5,208,488). Applicant respectfully traverses this rejection.

Independent claim 1 recites a method of protecting an integrated circuit from an over voltage comprised in part by "coupling the pad voltage to a bias for the integrated circuit when the power supply is below the predetermined value." Applicant respectfully submits that the cited reference does not disclose or suggest the recited element.

Rather, the potential detection circuit of Takiba is used to enable the read and write modes of an EPROM not to bias an integrated circuit. "To this end, a select signal Vpp is used, and the potential detecting circuit 52 which operates in response to the select signal is provided. In this case, such an operation of the potential detecting circuit suffices that it produces the VDD potential for the potential of the Vpp level, and produces ground potential for the input potential of the VDD level or less." (Takia, col. 6, lines 15-25). Thus the potential detection circuit of Takiba simply outputs a high (VDD) or low (ground) voltage level depending on the value of a select signal and does not disclose or suggest coupling a pad voltage to a IC bias.

Accordingly, applicant respectfully submits that claim 1 recites a novel and unobvious method over Takiba and is therefore allowable. Applicant further submits that claims 2-4 that depend directly or indirectly on claim 1 are allowable as is claim 1 and for additional limitations recited therein.

Independent claim 5 recites a method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (VDDO) is not present comprised in part by "providing bias-mid to an input electrode of the first semiconductor device such that the first semiconductor device will turn off when bias_mid - VDDO exceeds the threshold of the first semiconductor device; and actuating a switch in response to the turn off of the first semiconductor device to couple Vpad to bias_mid." Applicant respectfully submits that the cited reference does not disclose or suggest the recited element.

The Examiner alleges that N11 of Takiba reads on the first semiconductor device. Applicant respectfully traverses this rejection. The source of the NMOS transistor N11 of Takiba is grounded and is not coupled to a bias voltage bias_mid. Takiba, FIG. 2, col. 4, lines 1-3). In addition, turning off N11 does not actuate a switch to couple a pad voltage to bias_mid. Accordingly, applicant respectfully submits that claim 5 recites a novel and unobvious method over Takiba and is therefore allowable. Applicant further submits that claim 6 that depends directly or indirectly on claim 5 is allowable as is claim 5 and for additional limitations recited therein.

It is therefore respectfully submitted that pending claims 1-6 are in condition for allowance, and an early notice of allowance is respectfully requested.

Attached hereto is a marked-up version of the changes made to the above-identified application by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____

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626/795-9900

PAN/pan

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method of protecting an integrated circuit from over voltage, the method comprising:

accepting a voltage from a power supply input to the integrated circuit;

accepting a pad voltage from an external voltage source;

comparing the power supply voltage to a predetermined value; and

coupling [~~using~~] the pad voltage to [~~generate~~] a bias [~~voltage~~] for the integrated circuit when the power supply is below the predetermined value.

3. (Amended) A method as in claim 2 wherein using the pad voltage to generate a bias voltage for the integrated circuit further comprises [~~:~~

~~coupling the drain of the PMOS device to the pad voltage; and~~]

using the source voltage of the PMOS device to couple the pad voltage to the bias voltage.

4. (Amended) A method as in claim 2 wherein coupling the pad voltage into the drain of a PMOS (P-channel Metal Oxide Semiconductor) device comprises:

providing the pad voltage to an input of a plurality of diode connected MOS devices; and

coupling an output of the plurality of diode connected MOS devices to the drain of the PMOS device.

5. (Amended) A method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (V_{DDO}) is not present the method comprising:

providing V_{DDO} to a control electrode of a first semiconductor device;

providing [~~bias-mid~~] bias_mid to an input electrode of the first semiconductor device such that the first semiconductor device will

turn off when bias_mid - V_{DDO} exceeds the threshold of the first semiconductor device; and

actuating a switch in response to [~~using~~] the turn off of the first semiconductor device to couple Vpad to bias_mid.

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